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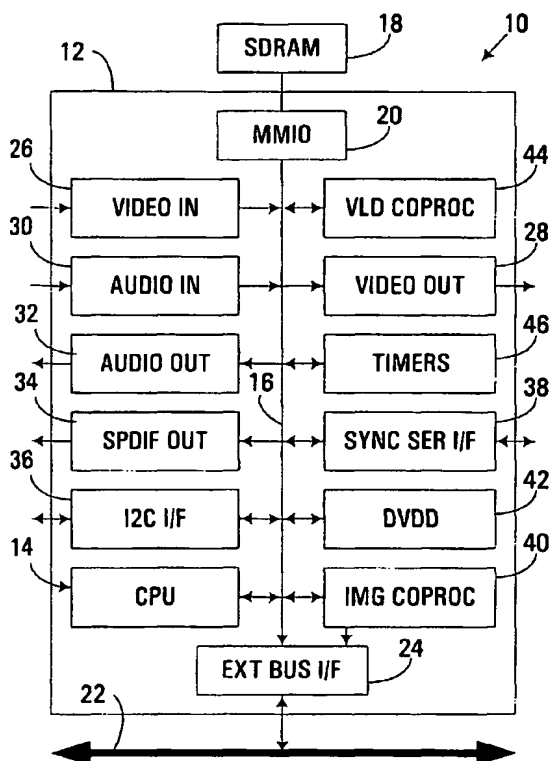
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[Continued on next page]

(54) Title: REGISTER FILE GATING TO REDUCE MICROPROCESSOR POWER DISSIPATION



(57) Abstract: A circuit arrangement and method of controlling power dissipation utilize a register file (60) with power dissipation control capabilities through a banked register design coupled with enable logic (62, 82) that is configured to selectively disable unused banks (70) of registers by selectively gating off clock (74), address (76) and data (78) inputs supplied thereto.



European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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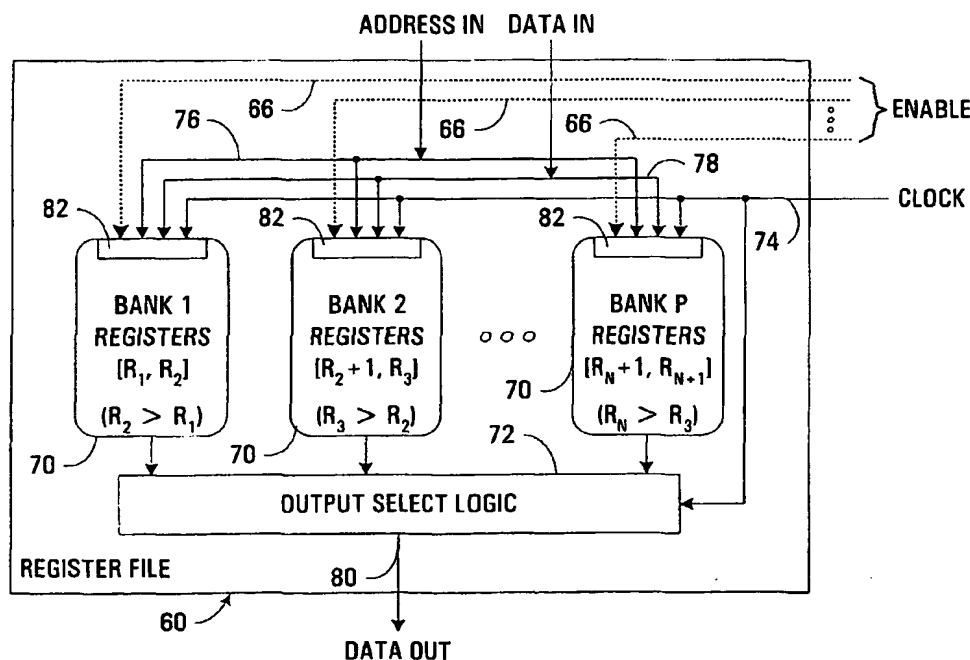
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